

WHAT IS CLAIMED IS:

1. A multi-protocol bus system, comprising:

2 a plurality of protocol indicators associated with an address
3 space, each of said plurality of protocol indicators associated
4 with a segment of said address space and configured to indicate a
5 particular bus protocol; and

6 a bus protocol selection subsystem configured to employ
7 control lines to implement one of said particular bus protocols in
8 accordance with a selected one of said protocol indicators based
upon an addressed segment of said address space.

2 2. The multi-protocol bus system as recited in Claim 1
further comprising a chip selection subsystem configured to provide
a chip selection signal to an external device based upon said
addressed segment of said address space.

3 3. The multi-protocol bus system as recited in Claim 2

2 wherein said external device is selected from the group consisting
3 of:

4 a fast pattern processor,

5 a routing switch processor,

6 a Motorola-style bus architecture device, and

7 an Intel-style bus architecture device.

4. The multi-protocol bus system as recited in Claim 1
2 wherein said particular bus protocol is selected from the group
3 consisting of:

4 a Motorola-style bus protocol, and
5 an Intel-style bus protocol.

5. The multi-protocol bus system as recited in Claim 1
2 wherein said control lines are selected from the group consisting
3 of:

4 an address latch enable control line,
a chip select control line,
a read data strobe control line,
a write data strobe control line,
a ready control line,
a read/write select control line,
a data strobe control line, and
a data acknowledge control line.

6. The multi-protocol bus system as recited in Claim 1
2 wherein each segment of said address space is four kilobytes.

7. The multi-protocol bus system as recited in Claim 1
2 wherein said address space is a peripheral component interconnect
3 (PCI) address space of thirty-two kilobytes.

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8. A method of operating a multi-protocol bus system,

2 comprising:

3 employing a plurality of protocol indicators associated with
4 an address space, each of said plurality of protocol indicators
5 associated with a segment of said address space and indicate a
6 particular bus protocol; and

7 employing control lines to implement one of said particular
8 bus protocols in accordance with a selected one of said protocol
9 indicators based upon an addressed segment of said address space.

9. The method as recited in Claim 8 further comprising
providing a chip selection signal to an external device with a chip
selection subsystem based upon said addressed segment of said
address space.

10. The method as recited in Claim 9 wherein said external
device is selected from the group consisting of:

3 a fast pattern processor,

4 a routing switch processor,

5 a Motorola-style bus architecture device, and

6 an Intel-style bus architecture device.

11. The method as recited in Claim 8 wherein said particular
2 bus protocol is selected from the group consisting of:
3 a Motorola-style bus protocol, and
4 an Intel-style bus protocol.

12. The method as recited in Claim 8 wherein said control
2 lines are selected from the group consisting of:
3 an address latch enable control line,
4 a chip select control line,
5 a read control line,
6 a write control line,
7 a ready control line,
8 a read/write control line,
9 a data strobe control line, and
10 a data acknowledge control line.

13. The method as recited in Claim 8 wherein each segment of
2 said address space is four kilobytes.

14. The method as recited in Claim 8 wherein said address
2 space is a peripheral component interconnect (PCI) address space of
3 thirty-two kilobytes.

15. A system interface processor, comprising:
2 a protocol data unit (PDU) receiver that receives PDUs;
3 a protocol data unit (PDU) transmitter that transmits PDUs;
4 and
5 a peripheral component interconnect (PCI) interface that
6 receives PDUs from said PDU receiver, transmits PDUs to said PDU
7 transmitter and interfaces with a multi-protocol bus, said PCI
8 interface including a multi-protocol bus system, having:
9 a plurality of protocol indicators associated with an
10 address space, each of said plurality of protocol indicators
11 associated with a segment of said address space and indicate
12 a particular bus protocol; and
13 a bus protocol selection subsystem that employs control
14 lines to implement one of said particular bus protocols in
15 accordance with a selected one of said protocol indicators
16 based upon an addressed segment of said address space.

16. The system interface processor as recited in Claim 15
2 wherein said multi-protocol bus system further includes a chip
3 selection subsystem that provides a chip selection signal to an
4 external device based upon said addressed segment of said address
5 space.

17. The system interface processor as recited in Claim 16

2 wherein said external device is selected from the group consisting

3 of:

4 a fast pattern processor,

5 a routing switch processor,

6 a Motorola-style bus architecture device, and

7 an Intel-style bus architecture device.

18. The system interface processor as recited in Claim 15

2 wherein said particular bus protocol is selected from the group

3 consisting of:

a Motorola-style bus protocol, and

an Intel-style bus protocol.

19. The system interface processor as recited in Claim 15

2 wherein said control lines are selected from the group consisting

3 of:

4 an address latch enable control line,

5 a chip select control line,

6 a read control line,

7 a write control line,

8 a ready control line,

9 a read/write control line,

10 a data strobe control line, and

11 a data acknowledge control line.

20. The system interface processor as recited in Claim 15
2 wherein each segment of said address space is four kilobytes.

21. The system interface processor as recited in Claim 15
2 wherein said address space is a peripheral component interconnect
3 (PCI) address space of thirty-two kilobytes.